layer **426**. The thickness is chosen so as to be substantially impervious to ion implantation being used in subsequent steps to form regions **66**, **86**, **67**, **87**, **68**, **88**, **69**, **89**, **89'** (see FIGS. **5-6**) where layer **426** also acts in part as an implant mask. In the embodiment shown, layer **426**, comprises spaced-apart portions **4261**, **4262**, **4263**, and **4264** with openings **4271**, **4272**, **4273**, **4274**, **4275** therein (collectively **427**). The locations and spacing of these various parts of layer **426** and openings **427** are chosen so that the location, width and spacing of N+ regions **87**, **89**. **89'** and P+ regions **86**, **88** (see FIGS. **6** and **19-20**) are determined by layer **426**, which acts as a single self-aligned mask. In this way, the location, width and spacing of N+ regions **87**, **89**, **89'** and P+ regions **86**, **88** do not depend upon high precision alignment of various subsequent implant or other dopant blocking masks. Since such N+ and P+ regions can be generally quite shallow (e.g., about ≦0.5 micrometers) silicide blocking layer **426** can be relatively thin since, in the preferred embodiment, the implants used to form such N+ and P+ regions are of comparatively low energy and have limited penetrating power. If higher energy and deeper penetration are desired or if other doping means are utilized to form such N+ and P+ regions, then the thickness of layer **426** is adjusted accordingly. Such adjustments are within the competence of those of skill in the art. Structure **317** results.

**[0033]** Referring now to manufacturing stage **218** of FIG. **18**, first selector mask **428** having openings **429** is applied over structure **317**. Openings **4271**, **4273**, **4275** in layer **426** are exposed in openings **429** of mask **428**. N+ regions **87**, **89**, **89'** are desirably formed by N type implant **430** to depth **872**, as desired by the device designer, where precision of the location, width and spacing of such N+ regions is determined by layer **426**. Structure **318** results. Referring now to manufacturing stage **219** of FIG. **19**, mask **428** is removed and second selector mask **432** having openings **433** is applied over structure **317**. Openings **4272** and **4274** in layer **426** are exposed in openings **433** of mask **432**. P+ regions **86** and **88** are desirably formed by P type implant **434** to depth **862**, as desired by the device designer, where the precision of location, width and spacing of such P+ regions is determined by layer **426**. Structure **319** results.

**[0034]** Referring now to manufacturing stage **220** of FIG. **20**, various conductive (e.g. metal or semimetal) vias and layers **438**, **440**, **442** and **444** with intervening insulating dielectric layer IDL**1** of thickness **435** and intervening insulating dielectric layer IDL**2** of thickness **436** are provided over surface **812** and layer **426** to accomplish the connections to the various N+, P+ regions and to resistive region **424** as described in connection with FIGS. **5** and **6**. Suitable values for the thicknesses of and choice of materials for IDL**1**, IDL**2** and vias and conductors **438-444** are within the competence of those of skill in the art and will depend on the particular process capabilities available in the manufacturing line being used to fabricate devices **60**, **80**. Conductor (e.g., metal or semi-metal or doped poly) layer **440** is customarily referred to as "metal-1" and conductor (e.g., metal or semi-metal or doped poly) layer **444** is customarily referred to as "metal-2". Referring now to both FIGS. **6** and **20**: (i) individual conductive vias **4381**, **4382** provide Ohmic electrical connections to resistive region **424** so as to form resistor **98**, and (ii) individual conductive via **4383** corresponds to connection **861**, via **4384** corresponds to connection **871**, via **4385** corresponds to connection **881** and via **4386** corresponds to connection **891** (connection **891** ' is omitted in FIG. **20** to avoid unduly cluttering the drawing). Portion **4402** of metal-1 conductor layer **440** connects vias **4382** and **4383** so as to couple one end of resistor **98** to contact **861** of P+ region **86**. Portion **4404** of metal-1 conductor layer **440** connects vias **4385**, **881** and **4386**, **891** so as to Ohmically couple P+ region **88** and N+ region **89** with a substantially low resistance connection. Via portion **4421** (with portion **4401** of metal-1) couples a second end of resistor **98** to metal-2 layer portion **4441** which is in turn coupled through via portion **4422**, portion **4403** of metal-1 layer **440** and via portion **4384** to N+ region **87**, as seen schematically in FIG. **6**. Metal-2 layer portion **4441** is coupled to GND **23**. Via portion **4423** couples metal-1 layer portion **4404** to metal-2 layer portion **4442** which is, in turn, coupled to I/O **22**. Structure **320** results. Structure **320** provides the various N and P regions and accomplishes the electrical connections illustrated schematically in FIGS. **5** and **6**.

**[0035]** According to a first embodiment, there is provided an electronic device (**10**) having a first terminal (**22**) and a second terminal (**23**), comprising, a circuit core (**24**) coupled between the first terminal (**22**) and the second terminal (**23**), and at least one voltage limiting device (**11**, **60**, **80**) coupled between the first terminal (**22**) and the second terminal (**23**), wherein the voltage limiting device (**11**, **60**, **80**) comprises, a first bipolar transistor (**70**, **90**) having an emitter (**67**, **87**) of a first conductivity type, a first base (**62**, **82**) of a second opposite conductivity type and of first base width (**74**, **94**), and a first collector (**64**, **84**) of the first conductivity type, and a second bipolar transistor (**72**, **92**) having a second emitter (**68**, **88**) of the second conductivity type, a second base (**64**, **84**) of the first conductivity type and second base width (**76**, **96**), and a second collector (**62**, **82**) of the second conductivity type, a first base resistance (**78**, **98**) coupled between the first emitter (**67**, **87**) and the first base (**62**, **82**), a second base resistance (**79**, **99**) coupled between the second emitter (**68**, **88**) and the second base (**64**, **84**), and wherein a PN junction (**65**, **85**) exits between the first base (**62**, **82**) and the second base (**64**, **84**), and wherein the first emitter (**67**, **87**) is coupled to the second terminal (**23**) and the second emitter (**68**, **88**) is coupled to the first terminal (**22**). According to a further embodiment, the first base resistance (**78**, **98**) is equal or greater than about 5000 Ohms. According to a still further embodiment, the second base resistance (**79**, **99**) is substantially a short circuit. According to a yet further embodiment, the second base (**64**, **84**) comprises a further region (**100**) having a doping density higher than a remainder of the second base (**64**, **84**). According to a still yet further embodiment, the first base (**62**, **82**) also serves as the second collector (**62**, **82**) and the second base (**64**, **84**) also serves as the first collector (**64**, **84**). According to a still yet further embodiment, a trigger voltage Vt**1** and a holding voltage Vh of the voltage limiting device (**11**, **60**, **80**) are substantially similar. According to another embodiment, at least one of the first base resistance (**78**, **98**) and the second base resistance (**79**, **99**) is a deposited material. According to a still another embodiment, at least one of the first base resistance (**78**, **98**) and the second base resistance (**79**, **99**) comprises a semiconductor.

**[0036]** According to a second embodiment, an electronic device (**10**) having a voltage limiting device (**11**, **60**, **80**) coupled between an input/output (I/O) terminal (**22**) and a common terminal (**23**) of the electronic device (**10**), comprises, a first bipolar transistor (**70**, **90**) having an emitter (**67**, **87**) of a first conductivity type, a base (**62**, **82**) of first base width (**74**, **94**) and of a second, opposite conductivity type with a more heavily doped contact region (**66**, **86**) of the second conductivity type, and a collector (**64**, **84**) of the first conductivity type with a more heavily doped contact region (**69**, **89**) of the first conductivity type, and a second bipolar (**72**, **92**) transistor partially merged with the first bipolar transistor and having an emitter (**68**, **88**) of the second conduc-